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10/039,368	01/03/2002	David Dice	SUN01-15(P6910)	1134

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,368	DICE, DAVID	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/3/02 and 3/4/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) __ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-23 and 25-30* is/are rejected.

7)☒ Claim(s) *10 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 23 and 24 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Note claim 23 can not depend from itself.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United

States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 12, 14, 15, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Jourdan et al. (U.S. Patent No. 6,438,673 B1) (hereafter referred to as Jourdan et al.'673).

Referring to claim 1, Jourdan et al.'673 discloses, as claimed, in a computerized device (such as a pipelined microprocessor, see Col. 3, lines 31-36), a method for controlling speculative execution of instructions (by the speculative access indication from AND 140 see Fig. 1, and col. 4, lines 13-26), the method comprising the steps of: detecting a multiaccess memory condition (the conditions of load buffer 100, and link table 120, see Fig. 1, such as a load buffer hit/miss, a link table hit/miss, and the confidence value stored in the hit buffer entry of the load buffer being greater than or equal to a predetermined threshold, see Col. 5, lines 7-12); setting a value (by the value of the speculative access indication set by AND 140 see Fig. 1, and col. 4, lines 13-26) of a speculation indicator based on the multiaccess memory condition; if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device

(when the value of the speculative access indication from AND 140, see Fig. 1, is not zero), allowing speculative execution of instructions (see col. 5, lines 7-12) in a processor in the computerized device; and if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device (when the value of the speculative access indication from AND 140, see Fig. 1, is zero), not allowing speculative execution of instructions (see col. 4, lines 13-26, and col. 5, lines 12-20) in the processor in the computerized device.

Referring to claim 15, Jourdan et al.'673 discloses, as claimed, a processor (such as a pipelined microprocessor, see Col. 3, lines 31-36) configured to control speculative execution of instructions in a computerized device, the processor comprising: an instruction orderer (such as the instruction issue unit or instruction dispatch unit in the pipelined microprocessor, see Col. 3, lines 31-36) configured to receive and order a set of instructions for execution based on a speculation indicator (the speculative access indication from AND 140 see Fig. 1, and col. 4, lines 13-26); an instruction executer (such as the function units or ALU in the pipelined microprocessor, see Col. 3, lines 31-36) coupled to the instruction orderer, the instruction executer configured to

execute instructions in the set of instructions according to an order indicated by the instruction orderer; a speculation indicator (the speculative access indication from AND 140 see Fig. 1, and col. 4, lines 13-26) configured to receive and maintain a value that indicates if speculative execution of instructions is allowed in the processor; and a speculative execution controller (including such as 110, 160, 130, and 140, see Fig. 1) coupled to at least one of the instruction orderer and the instruction executer and coupled to the speculation indicator, the speculative execution controller configured to: detect a multiaccess memory condition (the conditions of load buffer 100, and link table 120, see Fig. 1, such as a load buffer hit/miss, a link table hit/miss, and the confidence value stored in the hit buffer entry of the load buffer being greater than or equal to a predetermined threshold, see Col. 5, lines 7-12); set a value (by the value of the speculative access indication set by AND 140 see Fig. 1, and col. 4, lines 13-26) of a speculation indicator based on the multiaccess memory condition; if the value of the speculation indicator indicates that speculative execution of instructions is allowed in the computerized device (when the value of the speculative access indication from AND 140, see Fig. 1, is not zero), allow speculative execution of instructions (see col. 5, lines 7-12)

in the processor in a computerized device; and if the value of the speculation indicator indicates that speculative execution of instructions is not allowed in the computerized device (when the value of the speculative access indication from AND 140, see Fig. 1, is zero), not allow speculative execution of instructions (see col. 4, lines 13-26, and col. 5, lines 12-20) in the processor in the computerized device.

As to claims 12 and 26, Jourdan et al.'673 also discloses: detecting a change in the value of the speculation indicator (by the value of the speculative access indication set by AND 140 see Fig. 1, and col. 4, lines 13-26) from a value (when the value of the speculative access indication from AND 140, see Fig. 1, is not zero) indicating speculative execution of instructions is allowed in a processor in the computerized device to a value (when the value of the speculative access indication from AND 140, see Fig. 1, is zero) that indicates that speculative execution of instructions is not allowed in that processor in the computerized device (claim 12

As to claim 14, Jourdan et al.'673 also discloses: the step of executing instructions in the processor (such as a pipelined microprocessor, see Col. 3, lines 31-36) in the computerized device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-9, 11, 13, 16-23, 25, and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jourdan et al.'673 in view of Babaian et al. (U.S. Patent Application No. 2001/0042189 A1) (hereafter referred to as Babaian et al.'189).

Jourdan et al.'673 discloses the claimed invention except for: identifying a potential of a second processor to concurrently access the memory location (claims 2 and 16); comparing the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor to identify a page table entry associated with the second processor that references the memory location associated with the access to the page table entry by

the first processor (claims 3 and 17); detecting that a page table entry referenced by the access to the page table entry of the first processor matches a page table entry contained in a translation lookaside buffer associated with the second processor (claims 4 and 18); detecting that the page table entry accessed by the first processor matches a page table entry referenced by a memory management unit of the second processor (claims 5 and 19); detecting when at least two processors in the computerized device have a potential to execute instructions that reference locations within a shared page of memory (claims 6 and 20); comparing the first processor translation lookaside buffer reference to a set of translation lookaside buffer references associated with a second processor (claims 7 and 21); identifying when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one second processor (claims 8 and 22); the speculation indicator is associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device (claims 9 and 23); determining when at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory (claims 11 and 25); operating a multiprocessor

cache coherency protocol to detect when a processor in the computerized device accesses a page table entry (claims 13 and 27); detect a multiaccess memory condition between the first and second processors via the first interface (claim 28); an interconnection mechanism coupling the first processor, the second processor, the memory system (claim 29); and detecting a multiaccess memory condition between the first and second processors (claim 30).

Babaian et al.'189 discloses a computer system comprising: identifying a potential of a second processor (710-2, 710-3, or 710-4, see Fig. 7) to concurrently access the memory location (such as shared cache 790, see Fig. 7); comparing the content of the access to the page table entry of the first processor (710-1, see Fig. 7) to a set of page table entries (in the page table as mentioned in Col. 6, lines 6-7) associated with the second processor to identify a page table entry associated with the second processor (710-2, 710-3, or 710-4, see Fig. 7) that references the memory location associated with the access to the page table entry by the first processor (710-1, see Fig. 7); detecting that a page table entry (in the page table as mentioned in Col. 6, lines 6-7) referenced by the access to the page table entry of the first processor matches a page table entry contained in a translation lookaside buffer (TLB inside

MMU 712, as mentioned in Col. 6, lines 5-6) associated with the second processor (710-2, 710-3, or 710-4, see Fig. 7); detecting that the page table entry (in the page table as mentioned in Col. 6, lines 6-7) accessed by the first processor matches a page table entry referenced by a memory management unit (712, see Fig. 8) of the second processor (710-2, 710-3, or 710-4, see Fig. 7); detecting when at least two processors (710-1, 710-2, 710-3, and 710-4, see Fig. 7) in the computerized device have a potential to execute instructions that reference locations within a shared page of memory (such as shared cache 790, or main memory, see Fig. 7); comparing the first processor translation lookaside buffer (TLB inside MMU 712, as mentioned in Col. 6, lines 5-6) reference to a set of translation lookaside buffer (TLB inside MMU 712, as mentioned in Col. 6, lines 5-6) references associated with a second processor (710-2, 710-3, or 710-4, see Fig. 7); identifying when a translation lookaside buffer (TLB inside MMU 712, as mentioned in Col. 6, lines 5-6) span associated with a first processor overlaps a translation lookaside buffer (TLB inside MMU 712, as mentioned in Col. 6, lines 5-6) span associated with at least one second processor (claim 8); the speculation indicator is associated with a page table entry (in the page table as mentioned in Col. 6, lines 6-7) containing a reference to memory referenced by at

least one instruction operating on the processor in the computerized device; determining when at least two processors (710-2, 710-3, or 710-4, see Fig. 7) in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory (such as shared cache 790, or main memory, see Fig. 7); operating a multiprocessor cache coherency protocol (see Col. 4, lines 7-9) to detect when a processor in the computerized device accesses a page table entry (in the page table as mentioned in Col. 6, lines 6-7); detect a multiaccess memory (such as shared cache 790, or main memory, see Fig. 7) condition between the first (such as 710-1, see Fig. 7) and second processors (such as 710-2, 710-3, or 710-4, see Fig. 7) via the first interface (interprocess connect 780, see Fig. 7); an interconnection mechanism (interprocess connect 780, see Fig. 7) coupling the first processor (such as 710-1, see Fig. 7), the second processor (such as 710-2, 710-3, or 710-4, see Fig. 7), the memory system (claim 29); and detecting a multiaccess memory (such as shared cache 790, or main memory, see Fig. 7) condition between the first (such as 710-1, see Fig. 7) and second processors (such as 710-2, 710-3, or 710-4, see Fig. 7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Jourdan et

al.'673's system to comprise: identifying a potential of a second processor to concurrently access the memory location (claims 2 and 16); comparing the content of the access to the page table entry of the first processor to a set of page table entries associated with the second processor to identify a page table entry associated with the second processor that references the memory location associated with the access to the page table entry by the first processor (claims 3 and 17); detecting that a page table entry referenced by the access to the page table entry of the first processor matches a page table entry contained in a translation lookaside buffer associated with the second processor (claims 4 and 18); detecting that the page table entry accessed by the first processor matches a page table entry referenced by a memory management unit of the second processor (claims 5 and 19); detecting when at least two processors in the computerized device have a potential to execute instructions that reference locations within a shared page of memory (claims 6 and 20); comparing the first processor translation lookaside buffer reference to a set of translation lookaside buffer references associated with a second processor (claims 7 and 21); identifying when a translation lookaside buffer span associated with a first processor overlaps a translation lookaside buffer span associated with at least one

second processor (claims 8 and 22); the speculation indicator is associated with a page table entry containing a reference to memory referenced by at least one instruction operating on the processor in the computerized device (claims 9 and 23); determining when at least two processors in the computerized device do not have a potential to execute instructions that reference locations within a shared page of memory (claims 11 and 25); operating a multiprocessor cache coherency protocol to detect when a processor in the computerized device accesses a page table entry (claims 13 and 27); detect a multiaccess memory condition between the first and second processors via the first interface (claim 28); an interconnection mechanism coupling the first processor, the second processor, the memory system (claim 29); and detecting a multiaccess memory condition between the first and second processors (claim 30), as taught by Babaian et al.'189, in order to use virtual address for memory references and to increase the processing throughput using more than one processor for the Jourdan et al.'673's system.

Further, as shown in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977), to duplicate parts for multiple effects generally does not provide patentable weight to the claimed invention.

Allowable Subject Matter

6. Claims 10 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Chen et al.'130 discloses a cluster architecture multiprocessor system comprising a plurality of processors sharing a main memory and the other resources. Hussen'350 discloses system to dynamically control the out-of-order execution of Load/Store instructions. A store barrier cache history bit is used to dynamically predict whether or not a store violation is likely to occur.

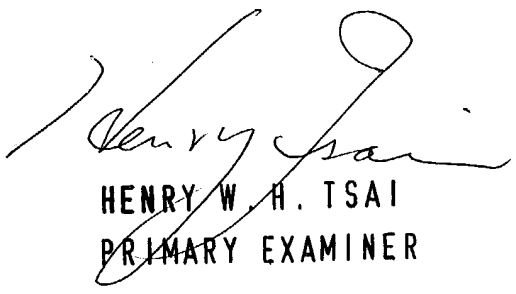
Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can

normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

9. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER
August 2, 2004